WHAT IS CLAIMED IS:

1. A ferroelectric memory comprising:

a memory cell array of memory cells having ferroelectric capacitors, which is divided into a plurality of blocks;

a first power switch of normally closed type connected to an external power terminal;

a power line, one end thereof being connected to said first power switch and the other end thereof being grounded via a first power capacitor;

a boost power circuit connected to said power line and provided in each said block of said memory cell array to generate a boost voltage required for operation of the memory;

a second power switch of normally open type connected in parallel to said boost power circuit and provided in each said block of said memory cell array;

a voltage detector circuit for detecting a drop of voltage level of said power line; and

a switch control circuit for turning on said second power switches in said blocks of said memory cell array excluding the second power switch in a currently selected block in response to said voltage detector circuit.

2. The ferroelectric memory according to claim 1, further comprising:

an internal power circuit supplied with the voltage of said power line to output an internal power voltage;

a second power capacitor between the voltage supply point and the ground; and

an internal power switch provided between said internal power circuit and said power line to be turned off under control of an output of said voltage detector circuit.

3. The ferroelectric memory according to claim 1, wherein said switch control circuit includes:

a block decoder for decoding an address signal and selecting a block from said memory cell array; and

a logical gate for controlling said first and second power switches and said internal power switch in accordance with a logic level of an output of said block decoder and a detection output of said voltage detector circuit.

4. The ferroelectric memory according to claim 3, wherein said switch control circuit selects said block in response to a block address from an address buffer for receiving an input address.

5. The ferroelectric memory according to claim 1, wherein said memory cell array includes a plurality of transistors connected in series between bit lines and plate lines individually and driven by different word lines, and ferroelectric capacitors connected in parallel with said transistors.

6. The ferroelectric memory according to claim 1, wherein a unit cell of said memory cell array comprises two transistors and two ferroelectric capacitors.

7. The ferroelectric memory according to claim 1, wherein a unit cell of said memory cell array comprises a transistor and a ferroelectric capacitor.